Fermilab

HRM-II MADC-64

6 Aug 2004

The MADC-64 card accepts 64 channels of analog inputs for digitization at rates of up to 160 Khz and provides 8 channels of analog output.

Byte-writes cannot be used when writing an MADC-64 through the HRM PMC; all writes must be word (16 bit) or long (32 bit).

Timestamp

A free-running 32-bit counter is clocked at 1 Mhz to provide a timestamp of 1 usec resolution. Timestamp data is acquired and travels with its corresponding channel samples. The timestamp is correlated to a TCLK event by the DSP on the HRM central board.

ADC Operation

Input channels are grouped in sets of 16 and presented to four DG506 multiplexers. The inputs have a +/-10v range and a nominal input resistance of 25k. ***There is no filtering on the inputs. Signal frequencies above $f_s/2$ must be attenuated at the source to avoid aliasing effects.*** The output of each mux drives an AD976 16-bit analog-to-digital converter. Sixty-four measurements are taken by the ADCs during each acquisition cycle of typically 100 usec. By manipulating the mux controls, these measurements can be distributed over all 64 inputs or over subsets of fewer channels to increase the sampling rate of a smaller number of inputs. Because acquisition is synchronous with the HRM DMA rate, slower sampling rates can be achieved by slowing the HRM DMA rate. A test mode feeds derived from the timestamp counter into the ADC datapath to verify the integrity of the entire HRM system, from the MADC card to the VME chassis. The ADCs are not accessible to the HRM DSP; ADC data streams directly to the HRM DMA channel.

DAC Operation

Two four-channel 16-bit digital-to-analog converters are mapped into DSP off-chip DM space. Their outputs are bipolar with 0x0 producing –5.000v and 0xFFFF producing +5.000v.

(The HRM DSP applies an offset so that the DACs appear to be 2s-complement at the PMC)

Scan Control Register Settings

Value	Mode	Active Channels	Sample Rate at

			10Khz DMA rate
0	64 channel	All	10 Khz
1	32 channel	0-7, 16-23, 32-39, 48-55	20 Khz
2	16 channel	0-3, 16-19, 32-35, 48-51	40 Khz
3	8 channel	0-1, 16-17, 32-33, 48-49	80 Khz
4	4 channel	0, 16, 32, 48	160 Khz
5	Test 0	Timestamp-derived data	NA
6	Test 1	Ramp	NA

Test mode 0 data formatting:

During test mode 0, the low 14 bits of the timestamp counter are inverted and routed into the data paths of the four ADCs. The ADCs fire rapidly in succession but then wait 6.25 usec until the next acquisition. ADC data will decrease 6 or 7 counts from channel to channel within a "quadrant" (channels 0-15, 16-31, 32-47, 48-63). Channels in different quadrant but having the same offset will have equal values. To guarantee that each channel has unique data, the top two bits (15:14) reflect their respective quadrant:

Channel	D[15:14]
0-15	00
16-31	01
32-47	10
48-63	11

D[13:08] = ~(TIMESTAMP[21:16])
D[07:00] = ~(TIMESTAMP[07:00])

Test mode 1 data formatting:

Data comes from a counter that increments with each ADC conversion. When data reaches 0xFFFF, the value wraps to 0x0040.

Channel_N_ data = Channel_(N-1)_ data +1

<u>HRM Central Board Address Space</u>

Base + 0x00 & Read
Module ID Register

15 8	7 0
Module ID = 0x72	Module Revision Number = 0x01

Base + 0x00 & Write
Module Typecodes Register

15 8	7 4	3 0
x	Timestamp TC	Data TC

Base + 0x01, Read/Write
Scan Control Register

15 3	2 0
x	Scan Ctrl

0 = 64ch (0-63)
1 = 32ch (0-7, 16-23, 32-39, 48-55)
2 = 16ch (0-3, 16-19, 32-35, 48-51)
3 = 8ch (0-1, 16-17, 32-33, 48-49)
4 = 4ch (0, 16, 32, 48)
5 = test

Base + 0x02, Read Only, Timestamp Low

15 0
Timestamp

Reading this register also latches the high word of the timestamp

Base + 0x03, Read Only, Timestamp High

15 0
Timestamp

Base + 0x04, Read Only, FPGA version

15 0
FPGA version

Base + 0x08 through 0x0F, Write Only
DAC0-7

15 0
DAC Data

0x0 = -5.000V, 0xFFFF = +5.000V

VME Address Space *(int and long int only)*

Base plus	Register
0x0, 0x1	Module ID
0x2, 0x3	Scan Control
0x4, 0x5	x
0x6, 0x7	x
0x8, 0x9	x
0xA, 0xB	Remote-unit-assigned data typecode
0xC, 0xD	Remote-unit-assigned timestamp typecode

0xE,0xF	x
0x10, 0x11	DAC0
0x12, 0x13	DAC1
0x14, 0x15	DAC2
0x16, 0x17	DAC3
0x18, 0x19	DAC4
0x1A, 0x1B	DAC5
0x1C, 0x1D	DAC6
0x1E, 0x1F	DAC7

Note:
DACs are restored at reset to the last written value. Uninitialized/reinitialized DACS are set to 0x8000 = 0.000v

DAC Connector Pinout
(A is the upper connector, B is the lower connector)

Pin Nr	P4A	P4B
1	DAC4	DAC0
2	DAC5	DAC1
3	DAC6	DAC2
4	DAC7	DAC3
5-9	AGND	AGND

ADC Connector Pinout
(A is the upper connector, B is the lower connector)

Pin Nr	P5A	P5B	P6A	P6B
1	Ch 32+	Ch 0+	Ch 48+	Ch 16+
2	Ch 33+	Ch 1+	Ch 49+	Ch 17+
3	Ch 34+	Ch 2+	Ch 50+	Ch 18+
4	Ch 35+	Ch 3+	Ch 51+	Ch 19+
5	Ch 36+	Ch 4+	Ch 52+	Ch 20+
6	Ch 37+	Ch 5+	Ch 53+	Ch 21+
7	Ch 38+	Ch 6+	Ch 54+	Ch 22+
8	Ch 39+	Ch 7+	Ch 55+	Ch 23+
9	Ch 40+	Ch 8+	Ch 56+	Ch 24+
10	Ch 41+	Ch 9+	Ch 57+	Ch 25+
11	Ch 42+	Ch 10+	Ch 58+	Ch 26+
12	Ch 43+	Ch 11+	Ch 59+	Ch 27+
13	Ch 44+	Ch 12+	Ch 60+	Ch 28+
14	Ch 45+	Ch 13+	Ch 61+	Ch 29+
15	Ch 46+	Ch 14+	Ch 62+	Ch 30+
16	Ch 47+	Ch 15+	Ch 63+	Ch 31+
17	(nc)	(nc)	(nc)	(nc)

18	(nc)	(nc)	(nc)	(nc)
19	(nc)	(nc)	(nc)	(nc)
20	Ch 32-	Ch 0-	Ch 48-	Ch 16-
21	Ch 33-	Ch 1-	Ch 49-	Ch 17-
22	Ch 34-	Ch 2-	Ch 50-	Ch 18-
23	Ch 35-	Ch 3-	Ch 51-	Ch 19-
24	Ch 36-	Ch 4-	Ch 52-	Ch 20-
25	Ch 37-	Ch 5-	Ch 53-	Ch 21-
26	Ch 38-	Ch 6-	Ch 54-	Ch 22-
27	Ch 39-	Ch 7-	Ch 55-	Ch 23-
28	Ch 40-	Ch 8-	Ch 56-	Ch 24-
29	Ch 41-	Ch 9-	Ch 57-	Ch 25-
30	Ch 42-	Ch 10-	Ch 58-	Ch 26-
31	Ch 43-	Ch 11-	Ch 59-	Ch 27-
32	Ch 44-	Ch 12-	Ch 60-	Ch 28-
33	Ch 45-	Ch 13-	Ch 61-	Ch 29-
34	Ch 46-	Ch 14-	Ch 62-	Ch 30-
35	Ch 47-	Ch 15-	Ch 63-	Ch 31-
36	AGND	AGND	AGND	AGND
37	AGND	AGND	AGND	AGND